EPC eGaN® FETs Reliability Testing: Phase 7

Chris Jakubiec, Rob Strittmatter Ph.D., and Chunhua Zhou Ph.D., Efficient Power Conversion Corporation , El Segundo, CA

Efficient Power Conversion (EPC) Corporation's enhancement-mode gallium nitride (eGaN®) FETs continue to expand into new market applications due to the competitive performance advantages over traditional power MOSFETs. Wireless power, DC-DC conversion, RF base station transmission, satellite systems, audio amplifiers, and LiDAR are just a few example applications that can take advantage of the superior performance of eGaN FETs.

Equally important is ensuring that eGaN FETs are intrinsically reliable within the intended applications. EPC's approach is to continually increase the amount of reliability test data statistics, further enhance the knowledge database, and prove that eGaN technology and products are a viable and dependable replacement solution to tradition silicon devices. In addition to a comprehensive review of results from previous reports, this Phase Seven Report includes new reliability data for intermittent operating life (IOL), early life failure rate (ELFR), electrostatic discharge (charge device model), and additional qualification of several products of the largest die size family and 300 V products.

The first section of this paper builds on the database of qualification data for eGaN FETs, including new data extending the product voltage range up to 300 V. Section II deals with the thermo-mechanical reliability of eGaN products' wafer level chip scale packaging, including recent temperature cycling (TC) and IOL data. Section III covers infant mortality testing on a large sample population, providing an upper bound on the early life failure rate. The last section will present reliability data in the field.

PART I: 40 V TO 300 V QUALIFICATION TESTING

Qualification Test Overview

The EPC2025 is the lead product extending the eGaN technology's voltage capability to 300 V. Reliability testing has concluded that the device parameters remain stable up to and including the 300 V device rating. Electrostatic discharge testing was also extended to cover the three standard industry models, Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). Additional reliability testing was completed on several of the largest die size products within the EPC product portfolio at the time of this report.

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature.
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature.
- High temperature storage (HTS): Parts are subjected to heat at the maximum rated temperature.
- Temperature cycling (TC): Parts are subjected to alternating high- and low temperature extremes.
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied.
- Unbiased autoclave (AC or Pressure Cooker Test): Parts are subjected to pressure, humidity, and temperature under condensing conditions.
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Electrostatic discharge (ESD): Parts are subjected to ESD under human body (HBM), machine (MM), and charged device (CDM) models.
- Intermittent operating life (IOL): Parts are subjected to an on/off cyclic DC power pulse which heats the device junction to a predefined temperature, and subsequently to an off state junction temperature.

The stability of the devices is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) standards [1] when possible.

Parts were mounted onto FR5 (high Tg FR4) or polyimide adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder [2] no clean flux was used in mounting the part onto an adaptor card.

Summary of Statistical Results

Table 1 summarizes reliability tests results and provides a composite statistical estimator of the failure rate. A combined total of over 7 million device-hours have been accumulated with zero failures. Since there are no failures, the statistic represents the worst case upper bound with 60% confidence. These upper bound values are limited only by the sample size, and will continue to drop as EPC continues to collect reliability data. For some stress tests where appropriate, both failures in time (FIT) and mean time to failure (MTTF) are calculated. These calculations assume an acceleration factor AF = 1. Therefore, operating under less stringent use conditions will yield an even lower projected rate of failure. For other stress tests, the failure rate (in ppm) is provided, along with the associated stress time period.

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (hrs)	Upper Bound Failure Statistic (60% Confidence)	Notes
HTRB	1754	0	2755000	333 FIT (MTTF = 343 yrs)	V_{DS} = 80% $V_{DS(max)}$
HTGB	1694	0	2695000	340 FIT (MTTF = 336 yrs)	$V_{GS} \geq 5.5$ V
TC	630	0	707000	1500 ppm	First 1000 cycles, $\Delta T \geq 100°C$
H3TRB	450	0	450000	2036 FIT (MTTF = 56 yrs)	—
ELFR HTRB	5966	0	286368	150 ppm	First 48 hrs
IOL	385	0	138600	NA	NA
All Tests	**10879**	**0**	**7031968**	—	—

Table 1. Summary of Composite Upper Bound Failure Statistics

High Temperature Reverse Bias

As part of the standard qualification, samples were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [3]. The part types on stress testing covered the full voltage range of 40 V to 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 x 2	3000
HTRB	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 x 3	2000
HTRB	EPC2032	100	XL (4.65 x 2.65)	T = 150°C, V_{DS} = 80 V	0	77 x 1	1000
HTRB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 80 V	0	77 x 1	1000
HTRB	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2024	40	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 32 V	0	60 x 1	1000
HTRB	EPC2023	30	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 24 V	0	77 x 1	1000
HTRB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 40 V	0	77 x 3	1000
HTRB	EPC2014C	40	M (1.70 x 1.09)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{DS} = 48 V	0	77 x 1	1000
HTRB	EPC2010C	200	L (3.55 x 1.63)	T = 150°C, V_{DS} = 160 V	0	77 x 2	3000
HTRB	EPC2012C	200	M (1.71 x 0.92)	T = 150°C, V_{DS} = 160 V	0	77 x 1	1000
HTRB	EPC2025	300	M (1.95 x 1.95)	T = 150°C, V_{DS} = 240 V	0	77 x 3	1000

Table 2. High Temperature Reverse Bias Test
Note: EPC800x results are applicable to all products in the EPC8000 series

The probability of failure based on the samples subjected to HTRB stress tests was estimated by calculating both failures in time (FIT) and mean time to failure (MTTF). Calculations assume: confidence level = 60%, acceleration factor (AF) = 1

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (Hrs)	FIT Rate	MTTF (Yrs)
HTRB	1754	0	2755000	333	343

Table 3. HTRB FIT and MTTF Calculation

High Temperature Gate Bias

Parts were subjected to 5.75 V or 5.5 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [3]. The part types on stress testing covered the full voltage range of 40 – 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, V_{DS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, V_{DS} = 5.75 V	0	77 x 3	2000
HTGB	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2023	30	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2038	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	1000
HTGB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 5.5 V	0	77 x 3	1000
HTGB	EPC2014C	40	M (1.70 x 1.09)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	2000
HTGB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 5.5 V	0	77 x 1	2000
HTGB	EPC2010C	200	L (3.55 x 1.63)	T = 150°C, V_{DS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2012C	200	M (1.71 x 0.92)	T = 150°C, V_{DS} = 5.75 V	0	77 x 1	1000
HTRB	EPC2025	300	M (1.95 x 1.95)	T = 150°C, V_{DS} = 240 V	0	77 x 3	1000

Table 4. High Temperature Gate Bias Test
Note: EPC800x results are applicable to all products in the EPC8000 series

The probability of failure based on the samples subjected to HTGB stress tests was estimated by calculating both failures in time (FIT) and mean time to failure (MTTF). Calculations assume: confidence level = 60%, acceleration factor (AF) = 1

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (Hrs)	FIT Rate	MTTF (Yrs)
HTGB	1694	0	2695000	340	336

Table 5. HTGB FIT and MTTF Calculation

High Temperature Storage

Parts were subjected to heat at the maximum rated temperature, in accordance with JEDEC Standard JESD22-A103 [4].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, Air	0	77 x 2	1000
HTS	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, Air	0	25 x 1	1000
HTS	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, Air	0	25 x 3	1000
HTS	EPC800x	40	S (2.05 x 0.85)	T = 150°C, Air	0	77 x 3	1000

Table 6. High Temperature Storage Test
Note: EPC800x results are applicable to all products in the EPC8000 series

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias at 85% RH and 85°C for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A101 [6].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2001C	100	L (4.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 1	1000
H3TRB	EPC2016C	100	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 2	1000
H3TRB	EPC2015	40	L (4.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	50 x 1	1000
H3TRB	EPC2010C	200	L (3.55 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50 x 1	1000
H3TRB	EPC2012	200	M (1.71 x 0.92)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50 x 1	1000
H3TRB	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	25 x 3	1000
H3TRB	EPC2033	150	XL (4.65 x 2.65)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	25 x 2	1000
H3TRB	EPC2029	80	XL (4.65 x 2.65)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	25 x 1	1000
H3TRB	EPC2022	100	XL (6.10 x 2.35)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	50 x 1, 25 x 1	1000

Table 7. High Temperature High Humidity Reverse Bias Test
Note: EPC800x results are applicable to all products in the EPC8000 series

The probability of failure based on the samples subjected to H3TRB stress tests was estimated by calculating both failures in time (FIT) and mean time to failure (MTTF). Calculations assume: confidence level = 60%, acceleration factor (AF) = 1

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (hrs)	FIT Rate	MTTF (Yrs)
H3TRB	450	0	450000	2036	56

Table 8. H3TRB FIT and MTTF Calculation

Autoclave (Unbiased Pressure Cooker)

Parts were subjected to 100% RH at 121°C under 29.7 PSIA vapor pressure for a stress period of 96 hours, in accordance with JEDEC Standard JESD22A-102 [7]. Devices were not electrically biased during stress.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
AC	EPC2001C	100	L (4.11 x 1.63)	T = 121°C, RH = 100%	0	25 x 1	96
AC	EPC2016C	100	M (2.11 x 1.63)	T = 121°C, RH = 100%	0	25 x 2	96

Table 9. Autoclave Test

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020 [8].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC2001C	100	L (4.11 x 1.63)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T=85°C, RH=85%, 3 reflow	0	25 x 1	168
MSL1	EPC2029	80	XL (4.65 x 2.65)	T=85°C, RH=85%, 3 reflow	0	25 x 2	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T=85°C, RH=85%, 3 reflow	0	77 x 3	168

Table 10. Moisture Sensitivity Level Test
Note: EPC800x results are applicable to all products in the EPC8000 series

Electrostatic Discharge

Parts were subjected to ESD HBM, MM, and CDM in accordance with the JEDEC Standard JESD22A-114 [9] Human Body Model, JESD22A-115 [10] Machine Model, and JESD22C-101 [11] Charged Device Model. EPC2001 and EPC800x were selected for the test to cover the die size range.

Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 400 V	(+) 500 V	1A
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 1500 V	(-) 2000 V	1C
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 200 V	(-) 400 V	B
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 400 V	(+) 600 V	C
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 600 V	—	> Class C

Table 11. Electrostatic Discharge Test EPC2001

Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 3000 V	(-) 4000 V	2
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 2000 V	(-) 3000 V	2
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
CDM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin - All Pins	(±) 1000 V	—	C3

Table 12. Electrostatic Discharge Test EPC2001C

Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 350 V	(-) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 350 V	(+) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 500 V	(+) 1000 V	1B
CDM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin - All Pins	(±) 500 V	(-) 500 V	1C
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 25V	(+) 50 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 100 V	(-) 200 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 50 V	(+) 100 V	A

Table 13. Electrostatic Discharge Test EPC800x
Note: EPC800x results are applicable to all products in the EPC8000 series

PART II: THERMO-MECHANICAL RELIABILITY

Thermo-Mechanical Testing

The rapid maturation of GaN power transistors continues to enable new capabilities in high frequency power conversion. eGaN devices in wafer level chip-scale packaging (WLCSP) have allowed the designer to harvest this higher speed performance due to the elimination of package-related parasitic inductance and thermal resistance. EPC continues to expand on the reliability evaluations of this package under thermo-mechanical stress. In addition to Temperature Cycling (TC) tests which have been included for all generations of eGaN devices, EPC has recently added an extensive Intermittent Operating Life (IOL) test capability. Results from both TC and IOL evaluations are provided below.

The main factor affecting the reliability during thermo-mechanical stress is the global coefficient of thermal expansion (CTE) mismatch of the die and PCB to which it is mounted. Because of the relatively large difference in CTE between the die (3 ppm/°C) and the PCB (~10-14 ppm/°C), shear strain will develop in the solder joints connecting the two. After a large number of temperature cycles, the repeated stress will cause fatigue and ultimately failure of the solder joint (see figure 1 for example).

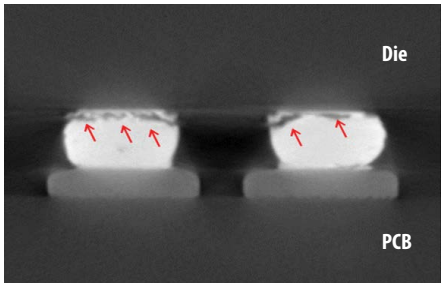

Figure 1: Severe cracking in solder joints on devices stressed to failure.

The thermo-mechanical shear strain in a solder joint can be estimated using the following simple equation:

$$\epsilon = \Delta\alpha * \Delta T \frac{DNP}{t}$$

where ε is the shear strain in the solder joint, Δα is the difference in CTE between die and PCB, ΔT is the temperature change during a cycle, DNP is the distance of the solder joint from the neutral point on the die, and t is the height of the solder joint. As a result, the joints that are farthest from the die center experience the most strain, and are therefore the first to fail. By increasing the bump height, TC/IOL reliability can be improved. Customers are encouraged to work with EPC to find an optimal bump solution for their application.

Temperature Cycling

Table 14 summarizes TC evaluations for multiple products ranging in size from small to extra-large. Parts were subjected to temperature cycling between either (-40°C and +125°C) or (0°C and +100°C) for a total of 1000 cycles or 1500 cycles respectively, in accordance with JEDEC Standard JESD22-A104 [5].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2001C	100	L (4.11 x 1.63)	-40 to +125°C, Air	0	35 x 3	1000
TC	EPC800x	40	S (2.05 x 0.85)	-40 to +125°C, Air	0	77 x 3	1000
TC	EPC800x	40	S (2.05 x 0.85)	-40 to +125°C, Air	0	35 x 1	1000
TC	EPC2021	80	XL (6.10 x 2.35)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2023	30	XL (6.10 x 2.35)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2029	80	XL (4.65 x 2.65)	-40 to +125°C, Air	0	35 x 2	1000
TC	EPC2010C	200	M (3.55 x 1.63)	-40 to +125°C, Air	0	35 x 1	1000

Table 14. Temperature Cycling Test
Note: EPC800x results are applicable to all products in the EPC8000 series

Though the TC tests listed in table 14 involve different products and different ΔT, we can merge the statistics to calculate a worst-case upper bound on the failure rate in the first 1000 cycles (with ΔT > = 100°C). The result is provided in table 15.

Stress Test	Sample Quantity	Fail Quantity	Equivalent Temp Cycles (ΔT >= 100°C)	Upper Bound Failure Rate (first 1000 cycles)
TC	630	0	707,000	1500 ppm

Table 15. Temperature Cycling FIT and MTTF Calculation

Intermittent Operating Life

Like TC, IOL subjects devices to cyclic temperature extremes. Instead of being heated by the ambient, however, they are self-heated by dissipating electrical power at the internal junction. The power level is tuned to achieve a predetermined temperature (Tj_{ON}) during the on phase. The power is subsequently reduced (or set to zero) to allow cooling back to the starting temperature (Tj_{OFF}) during the off phase. This cycle is repeated for thousands of iterations, with a typical cycle period of 4 minutes.

During IOL experiments, the parts are operated in the linear mode, with a near-threshold gate voltage in the range of 1 V to 2 V and a drain voltage of 4 V to 6 V. Op-amp feedback controls the gate, maintaining a specified current (and wattage) through the part (see fig. 2). The power set-point is computer controlled, and varies in time to provide a complete heating and cooling waveform over a 4 minute interval, with a cyclic temperature change ΔTj = 100°C. All parts undergo exactly the same cyclic waveform. Temperature is regularly monitored on the backside case of the die, using both an infrared camera and pyrometers. In both cases, the temperature sensors are close, but not in physical contact with the device under test. Figure 3 shows a typical thermal image of devices during the on state. During the ramp-down phase only, fans are used to cool the parts back to the ambient temperature at the start of each cycle. Power is monitored and logged on all parts continuously. Temperature is continuously logged (with a bank of pyrometers) on a subset of devices throughout the test duration.

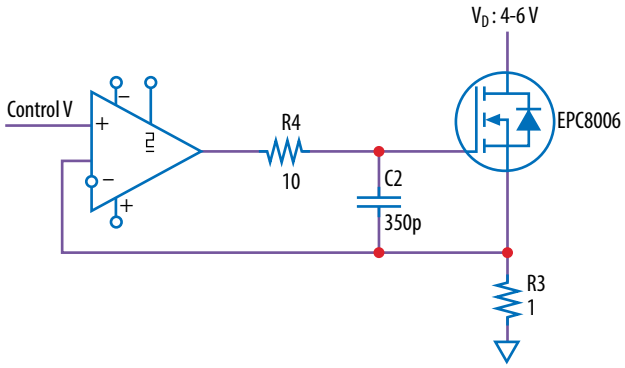

Figure 2: IOL test circuit. Power to the device is regulated using op-amp feedback.

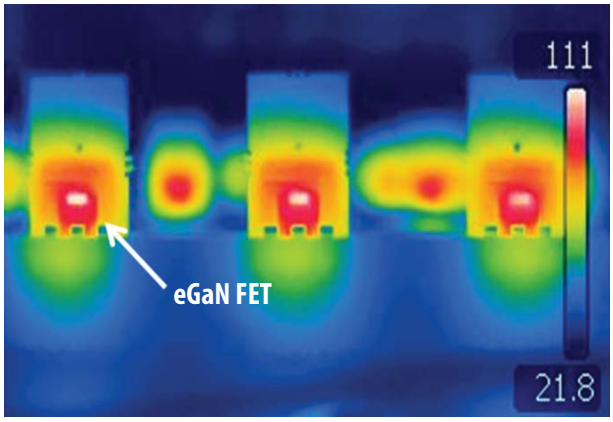

Figure 3: Thermal IR image of parts under IOL test. The FETs (white areas) are mounted to small rectangular PCBs during test.

To date, EPC has conducted IOL tests on three separate products that span the full range in die size for eGaN products (see table 16). In all cases, parts were mounted to PCB adapter cards (1.6 mm thick with 2 copper layers) using Kester NXG1 type 3 SAC305 solder. Units were then pre-conditioned following JEDEC JESD22-A113, which includes 3 reflow cycles at 260°C. Units were electrically pre-screened, as well as post-screened at multiple intervals throughout IOL testing to ensure all parameters were within datasheet specifications. Representative of EPC's family of small die, three lots of EPC800x were tested and all units passed the MIL-PRF-19500 [14] requirement of 6,000 cycles. One lot of a large die (EPC2001C) was also tested under the same conditions, and has passed 6000 cycles. One lot of the extra-large EPC2032 is also under test. This die represents the worst case for thermo-mechanical reliability of eGaN FETs, with the largest DNP values for the edge solder bumps. So far, this lot has passed 3000 cycles, with tests on-going.

EPC is continuing to accumulate TC and IOL data on multiple products in order to generate predictive models of solder joint fatigue failure under various operating conditions. These models will help our customers predict cycles to failure (Nf) in their target application and will be in our Phase 8 Report.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
IOL	EPC800x	40	S (2.05 x 0.85)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 3	6000
IOL	EPC2001C	100	L (4.11 x 1.63)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 1	6000
IOL	EPC2032	100	XL (4.65 x 2.65)	Tj_off = +40°C, Tj_on =+140°C, delta_Tj = 100°C	0	77 x 1	3000

Table 16. Intermittent Operating Life (IOL) Test Results

PART III: EVALUATING INFANT MORTALITY

Early Life Failure Rate

Early life failure rate (ELFR) or burn-in testing is a vital component in semiconductor device reliability testing. Referring to the well-known "bath-tub" curve shown in figure 4, ELFR testing seeks out failure modes that occur in the infant mortality region at the beginning of the device's operational life. These failure modes are caused by defects, usually arising from insufficient manufacturing controls or device screening.

ELFR testing requires a statistically significant sample size, stressed for a short duration (commonly between 48 and 168 hours). The output is the early life failure rate, typically quoted in parts per million (ppm), expressing the probability that a randomly chosen part will fail sometime during the specified infancy period.

In order establish very low ELFR, very large sample populations must be put to test. Consider, for example, a hypothetical product that contains a catastrophic defect affecting only one in a million parts (1 ppm). Even if the sample population were 100k parts, it would be unlikely to observe this failure mode even once. Acceleration factor tests would be of no help either. In this hypothetical case, the only statistically rigorous solution would be to test millions of parts. This is the basic reason why ELFR requires a large population. Though costly and labor intensive, ELFR testing provides unambiguous and invaluable reliability data for both EPC and its customers.

EPC has completed ELFR testing under HTRB stress using a large sample size (5966 units) of EPC2016C (medium sized 100 V FET). The stress conditions were 80 V V_{DS} at the maximum rated temperature (150°C) for a period of 48 hours. Following JESD47I [18] guidelines, samples were drawn from 4 nonconsecutive production lots, with no lot exceeding 40% of the population under test. Table 17 summarizes the test results.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	ELFR (upper bound 60% confidence)
HTRB_ELFR	EPC2016C	80	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	1610 x 1 1621 x 1 1614 x 1 1121 x 1	48	150 ppm

Table 17. HTRB ELFR

Since no failures occurred, the 60% upper confidence value for the failure rate (in the first 48 hours) is 150 ppm. This value was calculated based on χ2 statistics via the JEDEC standard 74A equation below [12]. (Note that using Gaussian statistics, a slightly lower value of 120 ppm is obtained [13]).

$$ELFR = \chi^2(\alpha, 2r+2)/(2*N)$$

where:

α: confidence level (60%)

r: total number of failures

$\chi^2(\alpha, 2r+2)$: Chi-square distribution factor (=1.83 for 60% confidence and 0 failures)

N: total number of device tested

The early life failure rate as calculated above is rooted in basic statistical principles, and its power is predicated on a large sample size. It does not require any assumptions about the underlying stochastic process of early failures, and it does not require any extrapolation using assumed acceleration factors. As a result, it takes on a certain statistical authority that is difficult to match using other test methodologies relying on relatively small sample sizes.

It is important to note that the ELFR of 150 ppm does not represent the true failure rate of EPC2016C over the first 48 hours. It is simply the minimum upper bound at 60% confidence, limited only by the size of the sample under test. Even so, the 150 ppm level represents a major milestone in the reliability testing of eGaN devices, setting a new bar for future testing. Achieving this failure rate requires strict process control, as well as rigorous screening and physical inspection of every device manufactured.

EPC is currently collecting infant mortality data under gate bias stress (HTGB) to be completed for the Phase 8 Report.

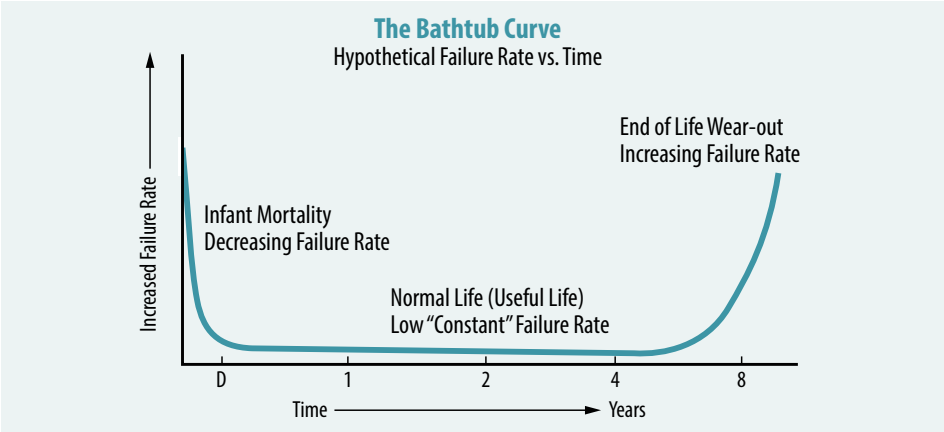

Figure 4: Hypothetical bathtub curve showing the stochastic failure rate throughout a product's operational life [from 15].

PART IV: FIELD RELIABILITY

Of utmost importance is how reliable eGaN FETs are while operating in customer applications. EPC monitors field reliability data to gauge reliability in customer applications. Over the past 6 years, we have tracked field returns and the total number of units deployed in the field. Figure 5 shows the distribution of accumulated field device hours amongst EPC different product families. At the time of this report (January 2016), over 17 billion total device hours have been tracked in the field.

Of the 127 total field returns during that time span, only 3 have been related to eGaN FETs failing within operating limits. The remaining failures were determined to be related to the assembly of the eGaN FETs or poor PCB layout (e.g. stray inductance in a circuit can lead to voltage overshoot). EPC has a trained engineering staff available to assist customers with both layout and assembly of eGaN devices.

Figure 6 shows the trend of FIT rate (Failures in 10^9 hours) for field reliability of all shipped eGaN products over the past 6 years. For these calculations, we assume that all products are deployed and remain in service from their original ship date. The values represent the upper bound on the FIT rate (at 60% confidence) based on the total accumulated device hours in the field, and the confirmed field failures [16].

Overall our field experience is approximately 0.24 FITs, which is at least comparable to silicon MOSFETs. Also, there is no evidence in the trend chart of an increased FIT rate in later years, which would suggest wear out over the 6 year span.

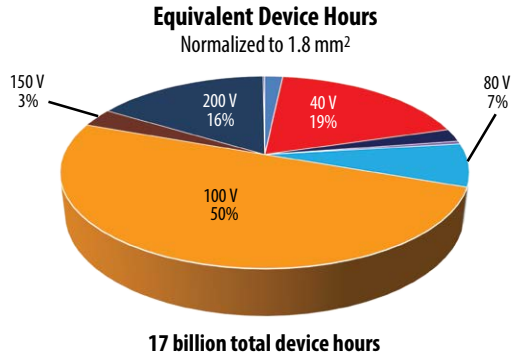

Figure 5: Pie chart showing the distribution of accumulated field device hours amongst EPC different product families.

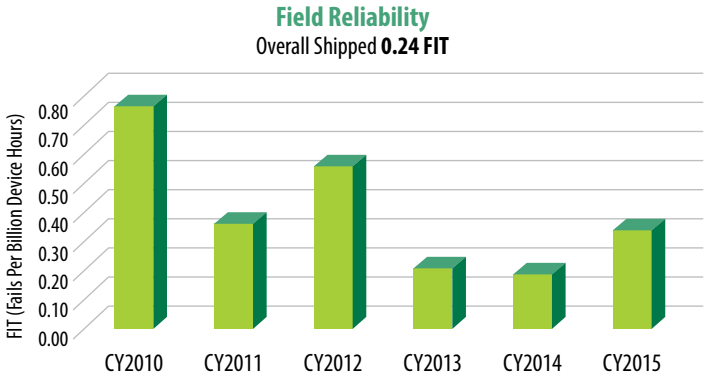

Figure 6: Field reliability trend chart for all deployed eGaN products over the past 6 years. Values represent 60% confidence upper bound on the FIT rate.

SUMMARY

In this Phase 7 report, we showed qualification data for new extra-large device and 300 V product offerings. We also reported on thermo-reliability evaluations, including for the first time IOL testing spanning the full range of device sizes. Using the largest sample size trial of eGaN FETs to date for infant mortality testing, we were able to obtain an upper bound ELFR of 150 ppm, demonstrating the effective process controls and screening methodologies in place for eGaN products. And finally, we reported a composite 0.24 FIT rate for products in the field. This value is consistent with all of our in situ evaluations to date, and shows that eGaN FETs have solid reliability.

In our next report (Phase 8), we plan to show qualification results on new products, including monolithic half-bridges and more extra-large devices. We will show extended ELFR test results, extending to new stress conditions and pooling data to create statistical "super-sets" with very large sample population. For thermo-mechanical reliability, we plan to provide a validated predictive model that will allow customers to estimate cycles to failure based on the die size, bump configuration, and stress conditions.

References

[1] https://www.jedec.org

[2] Kester NXG1 Lead-Free No-Clean Solder Paste Data Sheet Rev: 13Oct10

[3] JEDEC STANDARD Temperature, Bias, and Operating Life (https://www.jedec.org)

[4] JEDEC STANDARD High Temperature Storage Life (https://www.jedec.org)

[5] JEDEC STANDARD Temperature Cycling (https://www.jedec.org)

[6] JEDEC STANDARD Steady State Temperature Humidity Bias Life Test (https://www.jedec.org)

[7] JEDEC STANDARD Accelerated Moisture Resistance (https://www.jedec.org)

[8] IPC/JEDEC Joint Standard Moisture/Reflow (https://www.jedec.org)

[9] JEDEC STANDARD Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (https://www.jedec.org)

[10] JEDEC STANDARD Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (https://www.jedec.org)

[11] JEDEC STANDARD Electrostatic Discharge (ESD) Sensitivity Testing Charged Device Model (CDM) (https://www.jedec.org)

[12] JEDEC Standard No. 74A Early Life Failure Rate Calculation Procedure for Semiconductor Components (https://www.jedec.org)

[13] Edward Dudewicz and Satya Mishra, "Modern Mathematical Statistics", John Wiley and Sons, 1988.

[14] MIL-PRF-19500P Standard, "General Specifications for Semiconductor Devices", (http://www.everyspec.com)

[15] Dennis Wilkins, "The Bathtub Curve and Product Failure Behavior; Part One: The Bathtub Curve, Infant Mortality and Burn-in", Reliability HotWire eMagazine, Issue 21, November 2002.

[16] Arrhenius/FIT Rate Calculator, Maxim Integrated, https://www.maximintegrated.com/en/design/tools/calculators/general-engineering/qafits.cfm

[17] Alex Lidow, Johan Strydom, Michael de Rooij, David Reusch, "GaN Transistors for Efficient Power Conversion", Second Edition, John Wiley and Sons, 2015.

[18] JEDEC STANDARD Stress-Test-Driven Qualification of Integrated Circuits (https://www.jedec.org)